REMARKS

Specification

The disclosure was objected to because of informalities.

Accordingly, the specification has been amended to overcome the objection.

Rejections under 35 USC §112, Second Paragraph

Claim 1 was rejected under 35 USC §112, second paragraph, as being indefinite because "corresponding to a form position of said external connection terminal" allegedly was not clear.

Accordingly, the portion has been amended to "corresponding to a form position of said first external connection terminal" for clarification. Thus, the rejection has been overcome.

Rejections under 35 USC §102(b)

Claims 1-7 were rejected under 35 USC §102(b) as being anticipated by Kwon et al. (U.S. Patent No. 5,594,275).

Kwon et al discloses a semiconductor package having a plurality of stacked ball grid array packages. In Kwon et al, where a semiconductor package includes three substrates 61, 71, 81, the Examiner appears to consider the substrate 71 as the "third wiring substrate."

In order to clarify the present invention, claim 1 has been amended to recite, among other things, "a first external connection terminal provided at a surface opposite to a surface where said

semiconductor device is mounted of said first wiring substrate and a position facing a position at which said semiconductor device is mounted, and in the vicinity of said position facing said position at which said semiconductor device is mounted."

Explaining claim 1 using the example of FIG. 1, the first semiconductor device unit 11A and the second semiconductor device unit 12A are connected by the third wiring substrate 13A. Also, the external connection terminal 22 of the first semiconductor device unit 11A is situated at a position facing the mounting position of the first semiconductor element 14 and in the vicinity of the position. In the first semiconductor device unit 11A, the external connection terminal 22 is positioned on the mounting surface of the semiconductor element 14 and the position corresponding to the mounting position of the semiconductor element, so that the size of the semiconductor device is made small. Such a semiconductor device cannot be directly stacked on the second semiconductor device unit 12A.

The present invention realized the stacking of the first semiconductor device unit 11A on the second semiconductor device unit 12A by using the third wiring substrate 13A. As shown in an upper part of FIG. 1, the semiconductor device of a fan-in structure, where a connection terminal is provided in the central portion of the substrate, is stacked and combined on another semiconductor device so as to obtain a semiconductor device assembly to perform advanced functions.

On the other hand, according to Kwon et al, shown in FIG. 9, stacked circuit substrates 71, 81 and 91 have external connection members 76, 86 and 96 situated at the same positions.

Since a package 70 is mounted in the center of the substrate 71 situated at a middle step, the external connection member 86 is not provided at the back side of the position where the package 80 of the substrate 81 is mounted. Kwon et al does not teach or suggest that the first and second semiconductor device units are connected by the wiring substrate and that the external connection terminal of the first semiconductor device unit is situated at the position facing the mounting position of the first semiconductor device and in the vicinity of the position.

Thus, Kwon et al does not teach or suggest "a first external connection terminal provided at a surface opposite to a surface where said semiconductor device is mounted of said first wiring substrate and a position facing a position at which said semiconductor device is mounted, and in the vicinity of said position facing said position at which said semiconductor device is mounted" and "a third wiring, comprising a circuit board of said third wiring substrate arranged between said first semiconductor device unit and said second semiconductor device unit, a first conductive member for electrically connecting said circuit board and said connection electrode, a second conductive member that is formed corresponding to a form position of said first external connection terminal, said second conductive member being electrically connected to said first external connection terminal, and a third conductive member for electrically connecting said first conductive member and said second conductive member," as recited in claim 1.

For at least these reasons, claim 1 patentably distinguishes over Kwon et al. Claims 2-7, depending from claim 1, also patentably distinguish over Kwon et al for at least the same reasons.

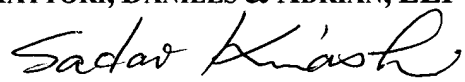
In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



Sadao Kinashi
Attorney for Applicants
Registration No. 48,075
Telephone: (202) 822-1100
Facsimile: (202) 822-1111

SK/sg

Q:\2004\042057\042057 amd 1.doc